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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/699,241
Filing Date	October 30, 2003
First Named Inventor	Michael Schlansker
Art Unit	2825
Examiner Name	Thuan V. Do
Attorney Docket Number	200300183-1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TD		US- 5,600,264-A	02-04-1997	Duong et al.	
TD		US- 4,670,749-A	06-02-1987	Freeman	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	10-28-2005

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TD		US- 5,631,578-A	05-20-1997	Clinton et al.	
TD		US- 5,651,013-A	07-22-1997	Iadanza	
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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300183-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Schlansker et al.		
	FILING DATE	GROUP 2825	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
TD	1A	6,204,690	Mar. 20, 2001	Young et al.	
TD	1B	6,243,851	Jun. 5, 2001	Hwang et al.	
TD	1C	6,292,022	Sep. 18, 2001	Young et al.	
TD	1D	6,553,395	Apr 22, 2003	Marshall et al.	
TD	1E	6,353,841	Mar. 5, 2003	Marshall et al.	
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

TD	1Q	V. Kathail, et al., PICO (Program In, Chip Out) : Automatically Designing Custom Computers, IEEE Computer, September 2002, 35(9), pp. 39-47.
TD	1R	S. C. Goldstein, et al., PipeRench: A Reconfigurable Architecture and Compiler, IEEE Computer, April 2000, 33(4).
TD	1S	S. C. Goldstein, et al., PipeRench: A Coprocessor for Streaming Multimedia Acceleration, In Proceedings of the 26th Annual International Symposium on Computer Architecture, 1999, pp. 28-39.

EXAMINER	DATE CONSIDERED
	10-28-2005

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	2A				
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

TD	2Q	V. Betz and J. Rose, Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency, IEEE Transactions on VLSI, Sept. 1998, 6(3), pp. 445-456.
TD	2R	Emre Özer, Sanjeev Banerjia, and Thomas M. Conte, Unified Assign and Schedule: A New Approach to Scheduling for Clustered Register File Microarchitectures, In Proceedings of the 31th Annual International Symposium on Microarchitecture (MICRO-31), Dallas, Texas, 1998, pp. 308-315.
TD	2S	M.C. Papaefthymiou, Understanding Retiming Through Maximum Average-Delay Cycles, Mathematical Systems Theory, 1994, 1(27), pp. 65-84.

EXAMINER	DATE CONSIDERED
Miranda	10-28-2005

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300183-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Schlansker et al.		
	FILING DATE	GROUP 2826	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
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		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

TD	3Q	J. Babb, R. Tessier, and A. Agarwal, Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators, In Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, Los Alamitos, CA 1993, pp. 142-151.
TD	3R	J.S. Rose and S. Brown, Flexibility of Interconnection Structures for Field-Programmable Gate Arrays, IEEE JSSC, March 1991, 26(3), pp. 277-282.
TD	3S	S. Note, et al., Cathedral III: Architecture driven high-level synthesis for high throughput DSP applications, In Proceedings of the 28th ACM/IEEE Design Automation Conference, DAC 91, San Francisco, CA, 1991, pp. 597 - 602.

EXAMINER	DATE CONSIDERED
Miranda	10-28-2005

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300183-1	APPLICATION NO.	CONFIRMATION NO.
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	FILING DATE	GROUP 1826	

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	4A				
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

TD	4Q	Constantine N. ANAGNOSTOPOULOS, Paul P. K. LEE, Application-Specific Integrated Circuits, The Electronics Handbook, pp. 731-748, CRC Press, Boca Raton FL, 1996.
TD	4R	Bradley K. FAWCETT, Software Development Tools for Field Programmable Gate Array Devices, The Electronics Handbook, pp. 784-793, CRC Press, Boca Raton FL, 1996.
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EXAMINER	DATE CONSIDERED
Nguyen	10-28-2005